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CHRISTIE, PARKER & HALE, LLP
P.O. BOX 7068
PASADENA, CA 91109-7068

EXAMINER	
POPHAM, JEFFREY D	

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,458	FUNG ET AL.	
	Examiner	Art Unit	
	Jeffrey D. Popham	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-18 and 20-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-18 and 20-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Remarks

Claims 1-4, 6-18, and 20-42 are pending.

Response to Arguments

1. Applicant's arguments filed 2/15/2006 have been fully considered but they are not persuasive.

Applicant argues that Nakaya does not process a second job until the first job is completed and the parallel processors are available. Nakaya teaches a multiple processor system in which multiple jobs and multiple portions of a single job (or both) can be processed in parallel. Figure 7 teaches the parallel processing of a single job. Figure 8 teaches the parallel processing of two jobs, in which each job has a dedicated serial processor, and there is one group of shared parallel processors. Within this embodiment, the serial processors will each process all serial instructions for its job, and when the job comes to a parallel processing portion, will request use of the shared group of parallel processors. If the shared group of parallel processors is in use by another job when the current job requests access, the current access request is queued and will be processed by the shared group of parallel processors once the other job's current use of the shared group is complete. While one job is using the shared group, the other job can still use its dedicated serial processor to perform serial processing on the data. Figure 26 and Column 34, lines 45-55 teach the parallel processing of multiple jobs, in which two jobs each have a dedicated serial processor and a group of

parallel processors. Both jobs can be processed at the same time, whether the current instructions are both serial, both parallel, or one serial and one parallel.

Regarding the cited sections of Nakaya, however, serial instructions are processed by a serial processor and parallel instructions are processed by parallel processors (as well as the serial processor). During parallel processing, a set of parallel instructions is processed and, when each processor completes processing, it will issue a termination notice. Each termination notice signifies that a certain parallel processor has completed processing of its instruction, and an interrupt will not be issued before all of the pertinent parallel processors' termination notices have been issued. Once all of the parallel processing is complete, the interrupt will be issued and the parallel processing of this set of parallel instructions is complete.

Applicant also argues that Nakaya does not disclose moving the second interrupt indicator onto the first interrupt indicator. As an example of how this occurs, claim 4 further defines moving the second interrupt indicator as comprising "delaying the generation of an interrupt associated with the younger control record." As is clear from the above discussion, this moving of the second interrupt indicator onto the first interrupt indicator is taught by Nakaya in that no interrupt will be issued until all of the parallel processors' termination notices have been issued.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 4, 6-14, 27, and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya (U.S. Patent 5,978,830) in view of Yamaura (U.S. Patent 6,175,890).

Regarding Claim 1,

Nakaya discloses a method for processing data using a plurality of processing engines, the method comprising:

Processing first data associated with an older control record in a first processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Issuing a first interrupt indicator (termination notice) when the processing of the first data is completed (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Processing second data associated with a younger control record in a second processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Issuing a second interrupt indicator (termination notice) when the processing of the second data is completed (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12); and

Moving the second interrupt indicator associated with the younger control record onto the first interrupt indicator associated with the older

control record if processing of the second data completes before processing of the first data (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not disclose the enablement of a first interrupt indicator in the older control record or a second interrupt indicator in the younger control record.

Yamaura, however, discloses enabling a first interrupt indicator associated with the older control record (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10); and

Enabling a second interrupt indicator associated with the younger control record (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Where the interrupt indicator is placed, whether it be in a register devoted to interrupt indicators and their associations to control records or within the control record itself, is of no significance to this method, since placing the interrupt indicator within the control record does not provide an advantage over using a register to store the indicator.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the parallel job schedule system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Regarding Claim 3,

Nakaya as modified by Yamaura discloses the method of claim 1, in addition Yamaura discloses that moving the second interrupt indicator comprises determining that the second interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Throughout this action, when the moving (or collapsing) of interrupt indicators is cited as being in Yamaura, it is to be understood that Yamaura teaches the foundations of how it is done, via the enabling and disabling of interrupt indicators within the interrupt controller, while the portion of Nakaya cited above discloses the moving of interrupt indicators (not issuing an interrupt until termination notices from all of the processors are issued).

Regarding Claim 4,

Nakaya as modified by Yamaura discloses the method of claim 1, in addition, Nakaya discloses that moving the second interrupt indicator comprises delaying the generation of an interrupt associated with the younger control record (Column 25, lines 40-63). The termination notices are issued at all of the processors before any one of the processors can generate the interrupt.

Regarding Claim 6,

Nakaya as modified by Yamaura discloses the method of claim 4, in addition, Yamaura discloses that moving the second interrupt indicator comprises setting the second interrupt indicator associated with the

younger control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 7,

Nakaya as modified by Yamaura discloses the method of claim 6, in addition, Yamaura discloses that moving the second interrupt indicator further comprises setting the first interrupt indicator associated with the older control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 8,

Nakaya as modified by Yamaura discloses the method of claim 1, in addition, Nakaya discloses that the older control record comprises a reference to data (Column 12, lines 13-29).

Regarding Claim 9,

Nakaya as modified by Yamaura discloses the method of claim 8, in addition, Nakaya discloses that the older control record comprises a reference to an operation to be performed on data (Column 12, lines 13-29).

Regarding Claim 10,

Nakaya as modified by Yamaura discloses the method of claim 1, in addition, Yamaura discloses writing processed data to memory associated with a host (Column 4, line 59 to Column 5, line 49).

Regarding Claim 11,

Nakaya as modified by Yamaura discloses the method of claim 10, in addition, Nakaya discloses that the processing engines are coupled to the interrupt controller (Figure 1); and Yamaura discloses that the external processor is coupled to the interrupt controller (Figure 1).

Regarding Claim 12,

Nakaya as modified by Yamaura discloses the method of claim 11, in addition, Nakaya discloses that the interrupt controller is coupled to the processing engines through a scheduler (synchronizer) (Figure 1).

Regarding Claim 13,

Nakaya as modified by Yamaura discloses the method of claim 12, in addition, Nakaya discloses generating an interrupt when processing of the older control record has been completed (Column 25, line 40 to Column 26, line 12).

Regarding Claim 14,

Nakaya as modified by Yamaura discloses the method of claim 13, in addition, Yamaura discloses that the external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

Regarding Claim 27,

Nakaya discloses a method for handling interrupts, comprising:

Receiving a first data block associated with a first interrupt indicator wherein the first interrupt indicator is configured to cause the generation of

a first interrupt upon completion of processing of the first data block (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Processing the first data block using a first processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Receiving a second data block associated with a second interrupt indicator wherein the second interrupt indicator is configured to cause the generation of a second interrupt upon completion of processing of the second data block (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Processing the second data block using a second processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12); and

Generating a single interrupt upon completion of processing of the first data block (the serial/parallel processor will generate a single interrupt upon completion of the parallel processing at all parts) (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not disclose setting interrupt indicators to enabled or determining if either of the first or second interrupt indicators are enabled.

Yamaura, however, discloses setting interrupt indicators to enabled and determining if any particular interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10). It would have been obvious to one of ordinary skill in the art at the time of applicant's

invention to incorporate the interrupt handling method of Yamaura into the parallel job schedule system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Regarding Claim 29,

Nakaya as modified by Yamaura discloses the method of claim 27, in addition, Nakaya discloses that the first data block is referenced in a first control record (Column 12, lines 13-29).

Regarding Claim 30,

Nakaya as modified by Yamaura discloses the method of claim 29, in addition, Nakaya discloses that the first control record contains information on an operation to perform on the first data block (Column 12, lines 13-29).

Regarding Claim 31,

Nakaya as modified by Yamaura discloses the method of claim 27, in addition, Nakaya discloses that the single interrupt is generated after processing of the first data block is completed (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12).

Regarding Claim 32,

Nakaya as modified by Yamaura discloses the method of claim 27, in addition, Nakaya discloses that the first interrupt indicator associated with the first data block is collapsed onto the second interrupt indicator

associated with the second data block (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12).

Regarding Claim 33,

Nakaya as modified by Yamaura discloses the method of claim 32, in addition, Yamaura discloses that collapsing the first interrupt indicator comprises setting the first interrupt indicator to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 34,

Nakaya as modified by Yamaura discloses the method of claim 33, in addition, Yamaura discloses that collapsing the first interrupt indicator comprises setting the second interrupt indicator to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

3. Claims 2, 15-18, 20-26, 28, and 35-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya in view of Yamaura, further in view of Pierson (Pierson et al., "Context-Agile Encryption for High Speed Communication Networks", Computer Communications Review, Association for Computing Machinery, Vol. 29, No. 1, January 1999, pp. 35-49).

Regarding Claim 2,

Nakaya in view of Yamaura does not disclose that the first processing engine is a public key engine.

Pierson, however, discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 28,

Nakaya in view of Yamaura does not disclose that the first and second processing engines are public key engines.

Pierson, however, discloses that the first and second processing engines are public key engines (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 15,

Nakaya discloses an apparatus, comprising:

A first processing engine configured to receive a first control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

A second processing engine configured to receive a second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

A history buffer (interrupt controller/synchronizer) containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12),

Wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not disclose that the apparatus is a cryptography accelerator; or an interface coupled to an external processor and memory associated with the external processor.

Yamaura, however, discloses an interface coupled to an external processor and memory associated with the external processor; the interface being coupled to the processing engines as well (Column 1, lines

12-30; Column 4, line 59 to Column 5, line 10; and Figure 1). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the parallel job schedule system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Pierson discloses that the apparatus is a cryptography accelerator (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 16,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 15, in addition, Pierson discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2).

Regarding Claim 17,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 15, in addition, Nakaya discloses that the history buffer is configured to collapse the first interrupt indicator associated with the first control record onto the second interrupt indicator associated with the

second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12), and Yamaura discloses that this is performed when the first interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 18,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 17, in addition, Nakaya discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises delaying the generation of an interrupt associated with the first control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12).

Regarding Claim 20,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 18, in addition, Yamaura discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the first interrupt indicator associated with the first control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 21,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 20, in addition, Yamaura discloses that collapsing the first interrupt indicator associated with the first control record onto the

second control record further comprises setting the second interrupt indicator associated with the second control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 22,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 15, in addition, Nakaya discloses that the second control record comprises a reference to data (Column 12, lines 13-29).

Regarding Claim 23,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 22, in addition, Nakaya discloses that the second control record comprises a reference to an operation to be performed on data (Column 12, lines 13-29).

Regarding Claim 24,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 23, in addition, Nakaya discloses that the external processor is coupled to the processing engines through a scheduler (synchronizer) (Figure 1).

Regarding Claim 25,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 24, in addition, Nakaya discloses that an interrupt is generated when processing of the second control record has been completed (Column 25, line 40 to Column 26, line 12).

Regarding Claim 26,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 25, in addition, Yamaura discloses that the external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

Regarding Claim 35,

Nakaya discloses an apparatus, comprising:

Means for receiving a first data block associated with a first interrupt indicator, wherein the first interrupt indicator is configured to cause the generation of a first interrupt upon completion of processing of the first data block (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Means for processing the first data block using a first processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Means for receiving a second data block associated with a second interrupt indicator, wherein the second interrupt indicator is configured to cause the generation of a second interrupt upon completion of processing of the second data block (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Means for processing the second data block using a second processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12); and

Means for generating a single interrupt upon completion of processing of the first data block (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not disclose that the apparatus is a cryptography device, or setting interrupt indicators to enabled or determining if either the first or second interrupt indicators are enabled.

Yamaura, however, discloses setting interrupt indicators to enabled and determining if any particular interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the parallel job schedule system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Pierson discloses that the apparatus is a cryptography device (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple

communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 36,

Nakaya as modified by Yamaura and Pierson disclose the device of claim 35, in addition, Pierson discloses that the first and second processing engines are public key engines (Pages 46-48, Section 5.2).

Regarding Claim 37,

Nakaya as modified by Yamaura and Pierson disclose the device of claim 35, in addition, Nakaya discloses that the first data block is referenced in a first control record (Column 12, lines 13-29).

Regarding Claim 38,

Nakaya as modified by Yamaura and Pierson disclose the device of claim 37, in addition, Nakaya discloses that the first control record contains information on an operation to perform on the first data block (Column 12, lines 13-29).

Regarding Claim 39,

Nakaya as modified by Yamaura and Pierson disclose the device of claim 35, in addition, Nakaya discloses that the single interrupt is generated after processing of the first data block is completed (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12).

Regarding Claim 40,

Nakaya as modified by Yamaura and Pierson disclose the device of claim 35, in addition, Nakaya discloses that the first interrupt indicator associated with the first data block is collapsed onto the second interrupt indicator associated with the second data block (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12).

Regarding Claim 41,

Nakaya as modified by Yamaura and Pierson disclose the device of claim 40, in addition, Yamaura disclose that collapsing the first interrupt indicator comprises setting the first interrupt indicator to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 42,

Nakaya as modified by Yamaura and Pierson disclose the device of claim 41, in addition, Yamaura discloses that collapsing the first interrupt indicator comprises setting the second interrupt indicator to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey D. Popham whose telephone number is (571)-272-7215. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey D Popham
Examiner
Art Unit 2137

EMMANUEL L. MOISE
SUPERVISORY PATENT EXAMINER